AMENDMENTS TO THE CLAIMS

Please amend claims 15, 16, 20 and 21 as follows.

1. (Original) A circuit, comprising:

a first control register to be loadable after the circuit is reset;

a first plurality of control registers to be loadable during an initialization process after the circuit is reset and to be unloadable until the circuit is reset again; and

a first switch unit coupled to the first control register and the first plurality of control registers, wherein the first switch unit to output data stored by one control register of the first plurality of control registers as a function of the data loaded in the first control register.

2. (Original) The circuit of claim 1, wherein the first switch unit comprises a multiplexer having input ports coupled to receive output from the first plurality of control registers and having a control port coupled to receive output from the first control register.

3. (Original) The circuit of claim 1, wherein the first control register is loadable through software control after the circuit is reset.

4. (Original) The circuit of claim 3, wherein the software control to cause the first register to be loaded with different data in response to a change in the circuit's operational mode.

5. (Original) The circuit of claim 1, wherein the circuit is a memory controller.

6. (Original) The circuit of claim 1, wherein the first plurality of control registers to be loaded by a basic input output system (BIOS) during an initialization process after the circuit is reset.

7. (Original) The circuit of claim 6, wherein the first plurality of control registers to be locked by the BIOS during the initialization process after the circuit is reset.

8. (Original) The circuit of claim 7, wherein the first plurality of control registers each include a lock bit to be set by the BIOS to lock the first plurality of control registers during the initialization process after the circuit is reset.

9. (Original) The circuit of claim 1, further comprising:

a second control register to be loadable after the circuit is reset;

a second plurality of control registers to be loadable during the initialization process and to be unloadable until the circuit is reset again; and

a second switch unit coupled to the second control register and the second plurality of control registers, wherein the second switch unit to output data stored by one control register of the second plurality of control registers as a function of the data loaded in the second control register.

10. (Original) A circuit, comprising:

means for storing first data and second data, the second data including a plurality of portions, wherein, after the circuit is reset and initialized the first data is changeable and the second data is not changeable; and

means for selecting one portion of the plurality of portions in response to the first data, wherein the selected portion to be provided to another unit of the circuit.

11. (Original) The circuit of claim 10, wherein the means for selecting comprises a multiplexer having input ports coupled to receive the second data and having a control port coupled to receive the first data.

12. (Original) The circuit of claim 10, wherein after the circuit is reset and initialized, the means for storing further for changing the first data in response to software control.

13. (Original) The circuit of claim 12, wherein the software control causes the first data to be changed in response to a change in the circuit's operational mode.

14. (Original) The circuit of claim 13, wherein the circuit's operational mode is user-selectable.

15. (Currently amended) The circuit of claim 10, wherein the means for storing is loadable with the ~~first~~ second data by a basic input output system (BIOS) during the initialization process.

16. (Currently amended) The circuit of claim 15, wherein the means for storing is locked by the BIOS to prevent changes to the ~~first~~ second data after the initialization process is performed, the ~~second~~ first data remaining changeable.

17. (Original) A method, comprising:

storing first data and second data in a circuit, the second data including a plurality of portions, wherein, after the circuit is reset and initialized, the first data is changeable and the second data is not changeable; and

selecting one portion of the plurality of portions in response to the first data, wherein the selected portion to be provided to another unit of the circuit.

18. (Original) The method of claim 17, further comprising changing the first data in response to software control.

19. (Original) The method of claim 18, wherein the software control causes the first data to be changed in response to a change in the circuit's operational mode.

20. (Currently amended) The method of claim 17, wherein storing ~~first~~ second data comprises:

storing the ~~first~~ second data by a basic input output system (BIOS) while the circuit is initialized.

21. (Currently amended) The method of claim 21, wherein the BIOS locks one or more control registers storing ~~first~~ second data to prevent changes to the ~~first~~ second data after the circuit is initialized.

22. (Original) A method, comprising:

loading a plurality of control registers of a circuit, the plurality of control registers including a plurality of protected registers and unprotected registers;

locking the plurality of protected control registers;

selecting a locked control register of the plurality of control registers; and

outputting data stored by the selected locked control register.

23. (Original) The method of claim 22, the locked control register is selected as a function of data stored in an unprotected control register of the plurality of control registers.

24. (Original) The method of claim 22, further comprising:

deselecting the locked control register; and

selecting another locked control register of the plurality of protected control registers.

25. (Original) An circuit, comprising:

a plurality of control registers;

means for loading the plurality of control registers, the plurality of control registers including a plurality of protected registers and unprotected registers;

means for locking the plurality of protected control registers;

means for selecting a locked control register of the plurality of control registers; and

means for outputting data stored by the selected locked control register.

26. (Original) The circuit of claim 25, wherein the means for selecting selects the locked control register as a function of data stored in an unprotected control register of the plurality of control registers.

27. (Original) The circuit of claim 25, further comprising:

means for deselecting the locked control register; and

means for selecting another locked control register of the plurality of protected control registers.

28. (Original) A system, comprising:

a processor;

a memory; and

a memory controller coupled to the processor and the memory, the memory controller comprising:

a first control register to be loadable after the memory controller is reset;

a first plurality of control registers to be loadable during an initialization process after the memory controller is reset and to be unloadable after initialization until the circuit is reset again; and

a first switch unit coupled to the first control register and the first plurality of control registers, wherein the first switch unit to output data stored by one control register of the first plurality of control registers as a function of the data loaded in the first control register.

29. (Original) The system of claim 28, wherein the first switch unit comprises a multiplexer having input ports coupled to receive output from the first plurality of control registers and having a control port coupled to receive output from the first control register.

30. (Original) The system of claim 28, wherein the first control register is loadable in response to software control after the circuit is initialized.